



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
[www.uspto.gov](http://www.uspto.gov)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/695,408	10/28/2003	Venkat Rangan	112-0122US	5639
29855	7590	10/18/2006	EXAMINER	
WONG, CABELLO, LUTSCH, RUTHERFORD & BRUCCULERI, L.L.P. 20333 SH 249 SUITE 600 HOUSTON, TX 77070			SUN, SCOTT C	
		ART UNIT	PAPER NUMBER	
		2182		

DATE MAILED: 10/18/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No.	Applicant(s)
	10/695,408	RANGAN ET AL.
	Examiner	Art Unit
	Scott Sun	2182

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### **Status**

- 1) Responsive to communication(s) filed on 19 July 2006.
- 2a) This action is **FINAL**.                            2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### **Disposition of Claims**

- 4) Claim(s) 1-36 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) Claim(s) \_\_\_\_\_ is/are allowed.
- 6) Claim(s) 1-36 is/are rejected.
- 7) Claim(s) \_\_\_\_\_ is/are objected to.
- 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### **Application Papers**

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### **Priority under 35 U.S.C. § 119**

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
 a) All    b) Some \* c) None of:
  1. Certified copies of the priority documents have been received.
  2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### **Attachment(s)**

1) <input type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)	5) <input type="checkbox"/> Notice of Informal Patent Application
Paper No(s)/Mail Date _____	6) <input type="checkbox"/> Other: _____

**DETAILED ACTION**

***Terminal Disclaimer***

1. The terminal disclaimer filed on 7/25/2006 disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of 10/695,435 has been reviewed and is accepted. The terminal disclaimer has been recorded.

***Response to Amendment***

2. Applicant's arguments filed 7/19/2006 have been fully considered but they are not persuasive. Applicant's arguments are summarized as:

- a. Prior art of record does not teach or suggest I/O module and control module "interactively" perform data migration.
- b. Prior art of record does not teach or suggest "delay" data write operations, but teaches "faulting" the operation instead.

2. Regarding argument 'a', examiner notes that the I/O module as disclosed by Edsall performs the basic data transfer functionalities (using connectors 302, 324; MAC 304, 322; and intercept switches 306 and 320), while Testardi teaches the higher-level functions of modifying table entries using the CP to configure a data migration. Therefore, the entire migration process would be completed using both the I/O module (for actual transfers of data being migrated) and the control module (for configuring metadata needed for the migration). As such, the combination of Edsall and Testardi

would result in the I/O module and the control module “interactively” performing data migration.

Examiner notes that this argument is further supported in teachings of Testardi, where an FP (fast-path) logic handles the basic I/O operations (paragraph 73) and the FP forwards higher-level functions such as data migration to the CP (control path) logic (paragraph 75; 135).

3. Regarding argument ‘b’, examiner notes that as applicant admits, Testardi teaches faulting to the CP results in the write operation “to be later retried”, or delayed. Although the particular method of delaying may be different from what applicant discloses in the specification (paragraph 222), it is noted that the specific features are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Examiner further notes that Testardi teaches that FP processes read operations to the barrier range, and faults write operations to the CP to be later retried (paragraph 207). This can be interpreted as FP delaying the write operations on the barrier range.

4. Having addressed each of applicant’s arguments, examiner notes that prior grounds of rejection still apply and are attached below. Minor changes are made to better clarify the rejection.

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Edsall et al (PG Pub #2003/0172149) in view of Testardi et al (PG Pub #2003/0140210).

7. Regarding claim 19, Edsall discloses a network (SAN, figure 1B) comprising:  
at least one host (hosts 144, 146) adapted to be connected to a switched fabric (switched fabric made up of switches 148, 150, 152; inter-switch links 154, 156; paragraphs 39, 40);

at least two storage units (storage devices 132-142) each adapted to be connected to a switched fabric (switches 148, 150, 152; inter-switch links 154, 156);  
a switched fabric (switches 148, 150, 152; inter-switch links 154, 156) connected to and coupling the at least one host and the at least two storage units (paragraph 39), the switched fabric comprising:

at least one switch (switches 148, 150, 152) for coupling to the at least one host and the at least two storage units; and  
a storage processing device (port processing logic in the switches, shown in figure 3A; paragraph 53) coupled to the at least one switch and for coupling to the at least one host and first and second storage units of the at least two storage units, where the first and second storage units may be directly connected

to the storage processing device or may be coupled through the at least one switch, the storage device including:

an input/output module (logic elements 302, 304, 306, 320, 322, 324) including processors to receive, operate on, and transmit network traffic (paragraph 53), and

Edsall does not disclose explicitly the storage processing device comprising a control module configured to perform data migration between the first and second storage units. However, Testardi discloses a switched fabric (element 20; figure 3; paragraph 64) comprising a storage processing device (distributed virtualization engines 34a-c) including a I/O module (fast paths) and a control module (control paths, paragraph 69) configured to interactively perform data migration (online-migration; paragraph 65, 66; details in figures 23, 24, paragraphs 204-212) between a first (physical volume p1) and a second storage device (physical volume p2). Examiner notes that fast paths handles basic I/O operations, and control path handles higher-level operations including migration (paragraphs 73, 75, 135). Teachings of Edsall and Testardi are from the same field of storage networks, and in particular using switched fabric to facilitate data operations.

Therefore, it would have been obvious at the time of invention for a person of ordinary skill in the art to combine teachings of Edsall with teachings of Testardi by implementing the data migration logic and data structures in the switched fabric system of Edsall for the benefit of efficient dispatch of data operations (in the instant case, data migration) to storage devices (Testardi, paragraph 9).

8. Regarding claim 20, Edsall and Testardi combined disclose claim 19, and Testardi further discloses wherein said processors include table information (figure 23, Rmap 560 and redirect tables) related to data migration (paragraph 204) and wherein said control module is coupled to said table information to maintain said table information for data migration (paragraph 206, 209).

9. Regarding claim 21, Edsall and Testardi combined disclose claim 20, and Testardi further discloses wherein table information includes a barrier entry (barrier range) and said processors delay data write operations if said barrier entry relates to said data write operation (paragraph 207).

10. Regarding claim 22, Edsall and Testardi combined disclose claim 20, and Testardi further discloses wherein said table information includes an entry (figure 23) related to the extents in the data migration, said entry defining an extent operation type (paragraph 204, 207).

11. Regarding claim 23, Edsall and Testardi combined disclose claim 22, and Testardi further discloses wherein said table information further includes a legend entry (rmap) for each extent operation type defining operations for the extent (paragraph 207).

12. Regarding claim 24, Edsall and Testardi combined disclose claim 23, and Testardi further discloses wherein said table information further includes entries referenced by said legend entry defining physical extent location. Examiner notes that the data migration is performed between two physical volumes, and therefore the table

information mapping extents in the migration operation reference physical locations of the extents.

13. Regarding claim 25, Edsall and Testardi combined disclose claim 24, and Testardi further discloses wherein legend entries include entries indicating data not migrated (entry value 1), data migrated (entry value 2), and a barrier entry for data being migrated (barrier range; read-only field 'r/o').

14. Regarding claim 26, Edsall and Testardi combined disclose claim 25, and Testardi further discloses wherein said processors delay data write operations if said barrier entry relates to said data write operations ("write operation faulted to CP to be later retried", paragraph 207).

15. Regarding claim 27, Edsall and Testardi combined disclose claim 26, and Testardi further discloses wherein said control module provides commands to copy data and places said barrier entry for said data being copied (paragraph 206).

16. Claims 1-18, 28-36 are substantially similar to claims 19-27 above. The same grounds for rejection are applied.

### ***Conclusion***

17. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

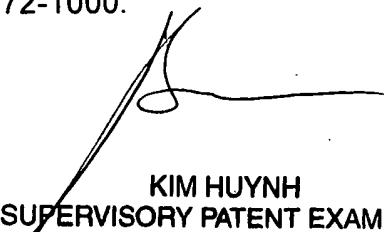
mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott Sun whose telephone number is (571) 272-2675. The examiner can normally be reached on M-F, 10:30am-7pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim N. Huynh can be reached on (571) 272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SS

  
KIM HUYNH  
SUPERVISORY PATENT EXAMINER

10/15/05